



TITLE OF THE INVENTION
HIGH FREQUENCY SIGNAL PEAK DETECTOR

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BACKGROUND OF THE INVENTION
TECHNICAL FIELD OF THE INVENTION

This invention relate generally to communication systems and more particularly to transmit power control within such communication systems.

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DESCRIPTION OF RELATED ART

Communication systems are known to support wireless and wire lined communications between wireless and/or wire lined communication devices. Such communication systems range from national and/or international cellular telephone systems to the Internet to point-to-point in-home wireless networks. Each type of communication system is constructed, and hence operates, in accordance with one or more communication standards. For instance, wireless communication systems may operate in accordance with one or more standards including, but not limited to, IEEE 802.11, Bluetooth, advanced mobile phone services (AMPS), digital AMPS, global system for mobile communications (GSM), code division multiple access (CDMA), local multi-point distribution systems (LMDS), multi-channel-multi-point distribution systems (MMDS), and/or variations thereof.

Depending on the type of wireless communication system, a wireless communication device, such as a cellular telephone, two-way radio, personal digital assistant (PDA), personal computer (PC), laptop computer, home entertainment equipment, et cetera communicates directly or indirectly with other wireless communication devices. For direct communications (also known as point-to-point communications), the participating wireless communication devices tune their receivers and transmitters to the same channel or channels (e.g., one of the plurality of radio frequency (RF) carriers of the wireless communication system) and communicate over that channel(s). For indirect wireless communications, each wireless communication

device communicates directly with an associated base station (e.g., for cellular services) and/or an associated access point (e.g., for an in-home or in-building wireless network) via an assigned channel. To complete a communication connection between the wireless communication devices, the associated base stations and/or associated access points
5 communicate with each other directly, via a system controller, via the public switch telephone network, via the Internet, and/or via some other wide area network.

For each wireless communication device to participate in wireless communications, it includes a built-in radio transceiver (i.e., receiver and transmitter) or
10 is coupled to an associated radio transceiver (e.g., a station for in-home and/or in-building wireless communication networks, RF modem, etc.). As is also known, the receiver is coupled to the antenna and includes a low noise amplifier, one or more intermediate frequency stages, a filtering stage, and a data recovery stage. The low noise amplifier receives inbound RF signals via the antenna and amplifies them. The one or more
15 intermediate frequency stages mix the amplified RF signals with one or more local oscillations to convert the amplified RF signal into baseband signals or intermediate frequency (IF) signals. The filtering stage filters the baseband signals or the IF signals to attenuate unwanted out of band signals to produce filtered signals. The data recovery stage recovers raw data from the filtered signals in accordance with the particular
20 wireless communication standard.

As is known, the transmitter includes a data modulation stage, one or more intermediate frequency stages, and a power amplifier. The data modulation stage converts raw data into baseband signals in accordance with a particular wireless
25 communication standard. The one or more intermediate frequency stages mix the baseband signals with one or more local oscillations to produce RF signals. The power amplifier amplifies the RF signals prior to transmission via an antenna.

The level at which the power amplifier amplifies the RF signals may be a fixed
30 level or varied. In many applications, it is desirable to be able to adjust the transmit power level of the power amplifier to conserve power when less power will suffice.

Typically, a lower transmit power may be used when the receiver that receives the signals of the transmitter receives the signals with a high received signal strength indication. In this instance, based on an indication of the peak value of the signal, the transmitter may reduce its transmit power level. To facilitate the transmit power level adjustment, the
5 transmitter includes a peak detection circuit.

While there are many ways in which a peak detection circuit may be implemented, when the peak detection circuit is implemented on an integrated circuit, there is a further need for simplification of circuitry with improved performance.
10 Further, measuring the peak detection of a single-ended signal is done using one type of peak detection circuit, while measuring the peak of a differential signal is done using a different type of peak detection circuit. Still further, as the rate of the signal increases (e.g., into the Giga Hertz range), peak detection circuits become less accurate due to the speed and/or become more complex.

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Therefore, a need exists for an accurate, flexible (e.g., handles single-ended and differential signals equally well), and compact peak detection circuit.

BRIEF SUMMARY OF THE INVENTION

20 The high frequency signal peak detection circuit of the present invention substantially meets these needs and others. In one embodiment, a signal power detector includes an input coupling circuit and a rectifying operational amplifier. The input coupling circuit is operably coupled to receive a signal and to convert the signal into a first input and a rectifying input. The rectifying operational amplifier is operably coupled
25 to receive the first input and the rectifying input and to produce therefrom a rectified output signal that represents a peak of the received signal. Such a high frequency signal peak detection circuit provides an accurate, flexible, and compact peak detect circuit.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

30 Figure 1 is a schematic block diagram of a wireless communication system in accordance with the present invention;

Figure 2 is a schematic block diagram of a wireless communication device in accordance with the present invention;

5 Figure 3 is a schematic block diagram of a signal peak detection circuit in accordance with the present invention;

Figure 4 is a schematic block diagram of another signal peak detection circuit in accordance with the present invention;

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Figure 5 is a schematic block diagram of yet another signal peak detection circuit in accordance with the present invention;

Figure 6 is a signal diagram of operation of the signal peak detection circuit of
15 Figure 4; and

Figure 7 is a signal diagram of operation of the signal peak detection circuit of Figure 5.

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DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a schematic block diagram illustrating a communication system 10 that includes a plurality of base stations and/or access points 12-16, a plurality of wireless communication devices 18-32 and a network hardware component 34. The wireless communication devices 18-32 may be laptop host computers 18 and 26, personal digital
25 assistant hosts 20 and 30, personal computer hosts 24 and 32 and/or cellular telephone hosts 22 and 28. The details of the wireless communication devices will be described in greater detail with reference to Figure 2.

The base stations or access points 12-16 are operably coupled to the network
30 hardware 34 via local area network connections 36, 38 and 40. The network hardware 34, which may be a router, switch, bridge, modem, system controller, et cetera provides a

wide area network connection 42 for the communication system 10. Each of the base stations or access points 12-16 has an associated antenna or antenna array to communicate with the wireless communication devices in its area. Typically, the wireless communication devices register with a particular base station or access point 12-14 to receive services from the communication system 10. For direct connections (i.e., point-to-point communications), wireless communication devices communicate directly via an allocated channel.

Typically, base stations are used for cellular telephone systems and like-type systems, while access points are used for in-home or in-building wireless networks. Regardless of the particular type of communication system, each wireless communication device includes a built-in radio and/or is coupled to a radio. The radio includes a highly linear amplifier and/or programmable multi-stage amplifier as disclosed herein to enhance performance, reduce costs, reduce size, and/or enhance broadband applications.

Figure 2 is a schematic block diagram illustrating a wireless communication device that includes the host device 18-32 and an associated radio 60. For cellular telephone hosts, the radio 60 is a built-in component. For personal digital assistants hosts, laptop hosts, and/or personal computer hosts, the radio 60 may be built-in or an externally coupled component.

As illustrated, the host device 18-32 includes a processing module 50, memory 52, radio interface 54, input interface 58 and output interface 56. The processing module 50 and memory 52 execute the corresponding instructions that are typically done by the host device. For example, for a cellular telephone host device, the processing module 50 performs the corresponding communication functions in accordance with a particular cellular telephone standard.

The radio interface 54 allows data to be received from and sent to the radio 60. For data received from the radio 60 (e.g., inbound data), the radio interface 54 provides the data to the processing module 50 for further processing and/or routing to the output

interface 56. The output interface 56 provides connectivity to an output display device such as a display, monitor, speakers, et cetera such that the received data may be displayed. The radio interface 54 also provides data from the processing module 50 to the radio 60. The processing module 50 may receive the outbound data from an input
5 device such as a keyboard, keypad, microphone, et cetera via the input interface 58 or generate the data itself. For data received via the input interface 58, the processing module 50 may perform a corresponding host function on the data and/or route it to the radio 60 via the radio interface 54.

10 Radio 60 includes a host interface 62, digital receiver processing module 64, an analog-to-digital converter 66, a filtering/gain module 68, an IF mixing down conversion stage 70, a receiver filter 71, a low noise amplifier 72, a transmitter/receiver switch 73, a local oscillation module 74, memory 75, a digital transmitter processing module 76, a digital-to-analog converter 78, a filtering/gain module 80, an IF mixing up conversion
15 stage 82, a power amplifier 84, a transmitter filter module 85, a signal peak detection circuit 95, and an antenna 86. The antenna 86 may be a single antenna that is shared by the transmit and receive paths as regulated by the Tx/Rx switch 73, or may include separate antennas for the transmit path and receive path. The antenna implementation will depend on the particular standard to which the wireless communication device is
20 compliant.

The digital receiver processing module 64 and the digital transmitter processing module 76, in combination with operational instructions stored in memory 75, execute digital receiver functions and digital transmitter functions, respectively. The digital
25 receiver functions include, but are not limited to, digital intermediate frequency to baseband conversion, demodulation, constellation demapping, decoding, and/or descrambling. The digital transmitter functions include, but are not limited to, scrambling, encoding, constellation mapping, modulation, and/or digital baseband to IF conversion. The digital receiver and transmitter processing modules 64 and 76 may be
30 implemented using a shared processing device, individual processing devices, or a plurality of processing devices. Such a processing device may be a microprocessor,

micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, analog circuitry, digital circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions. The memory 75 may be a single
5 memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, volatile memory, non-volatile memory, static memory, dynamic memory, flash memory, and/or any device that stores digital information. Note that when the processing module 64 and/or 76 implements one or more of its functions via a state machine, analog circuitry, digital circuitry, and/or logic
10 circuitry, the memory storing the corresponding operational instructions is embedded with the circuitry comprising the state machine, analog circuitry, digital circuitry, and/or logic circuitry.

In operation, the radio 60 receives outbound data 94 from the host device via the
15 host interface 62. The host interface 62 routes the outbound data 94 to the digital transmitter processing module 76, which processes the outbound data 94 in accordance with a particular wireless communication standard (e.g., IEEE 802.11 Bluetooth, et cetera) to produce digital transmission formatted data 96. The digital transmission formatted data 96 will be a digital base-band signal or a digital low IF signal, where the
20 low IF typically will be in the frequency range of one hundred kilohertz to a few megahertz.

The digital-to-analog converter 78 converts the digital transmission formatted data 96 from the digital domain to the analog domain. The filtering/gain module 80
25 filters and/or adjusts the gain of the analog signal prior to providing it to the IF mixing stage 82. The IF mixing stage 82 converts the analog baseband or low IF signal into an RF signal based on a transmitter local oscillation 83 provided by local oscillation module 74. The power amplifier 84 amplifies the RF signal to produce outbound RF signal 98, which is filtered by the transmitter filter module 85. The antenna 86 transmits the
30 outbound RF signal 98 to a targeted device such as a base station, an access point and/or another wireless communication device.

The signal peak detection circuit 95 is operably coupled to measure the peak of the outbound RF signals 98, wherein the peak value may be used to adjust the transmit power levels. In one embodiment, the signal peak detection circuit 95 measures the outbound RF signals 98 as single-ended signals at the T/R switch module 73. Such an embodiment will be described in greater detail with reference to Figures 3, 4, and 6. In another embodiment, the signal peak detection circuit 95 measures the outbound RF signals 98 as differential signals at the output of the power amplifier 84 or at the output of the TX filter module 85. Such an embodiment will be described in greater detail with reference to Figures 3, 5, and 7.

The radio 60 also receives an inbound RF signal 88 via the antenna 86, which was transmitted by a base station, an access point, or another wireless communication device. The antenna 86 provides the inbound RF signal 88 to the receiver filter module 71 via the Tx/Rx switch 73, where the Rx filter 71 bandpass filters the inbound RF signal 88. The Rx filter 71 provides the filtered RF signal to low noise amplifier 72, which amplifies the signal 88 to produce an amplified inbound RF signal. The low noise amplifier 72 provides the amplified inbound RF signal to the IF mixing module 70, which directly converts the amplified inbound RF signal into an inbound low IF signal or baseband signal based on a receiver local oscillation 81 provided by local oscillation module 74. The down conversion module 70 provides the inbound low IF signal or baseband signal to the filtering/gain module 68. The filtering/gain module 68 filters and/or gains the inbound low IF signal or the inbound baseband signal to produce a filtered inbound signal.

The analog-to-digital converter 66 converts the filtered inbound signal from the analog domain to the digital domain to produce digital reception formatted data 90. The digital receiver processing module 64 decodes, descrambles, demaps, and/or demodulates the digital reception formatted data 90 to recapture inbound data 92 in accordance with the particular wireless communication standard being implemented by radio 60. The host

interface 62 provides the recaptured inbound data 92 to the host device 18-32 via the radio interface 54.

As one of average skill in the art will appreciate, the wireless communication device of figure 2 may be implemented using one or more integrated circuits. For example, the host device may be implemented on one integrated circuit, the digital receiver processing module 64, the digital transmitter processing module 76 and memory 75 may be implemented on a second integrated circuit, and the remaining components of the radio 60, less the antenna 86, may be implemented on a third integrated circuit. As an alternate example, the radio 60 may be implemented on a single integrated circuit. As yet another example, the processing module 50 of the host device and the digital receiver and transmitter processing modules 64 and 76 may be a common processing device implemented on a single integrated circuit. Further, the memory 52 and memory 75 may be implemented on a single integrated circuit and/or on the same integrated circuit as the common processing modules of processing module 50 and the digital receiver and transmitter processing module 64 and 76.

Figure 3 is a schematic block diagram of the signal peak detection circuit 95 that includes an input coupling circuit 100 and a rectifying operational amplifier 102. The rectifying operational amplifier 102 includes first input transistor (T_{input_1}), a second input transistor (T_{input_2}), a rectifying transistor ($T_{rectify}$), a current source ($T_{current_source}$), first active input load transistor ($T_{input_load_1}$), a second active input load transistor ($T_{input_load_2}$), an output load transistor (T_{output_load}) and an output transconductance stage 118.

The input coupling circuit 100 receives a signal 108, which may be the outbound RF signals 98, and produces therefrom a first input 110 and a rectified input 112. In addition, the input coupling circuit 100 scales the signal 108 to ensure that the resulting signal strength indication is within a desired voltage range, which may be established based on an input range of an analog to digital converter. The analog to digital converter converts the resulting signal strength indication into a digital signal for processing by the digital section of the radio 60. Note that the signal 108 may be a single-ended signal or a

differential signal. When the signal 108 is a single-ended signal, the input coupling circuit 100 may be configured as shown in Figure 4. When the signal 108 is a differential signal, the input coupling circuit 100 may be configured as shown in Figure 5.

5 The first input transistor (T_{input_1}) receives the first input 110 and the rectifying transistor (T_{rectify}) receives the rectified input 112. The gate of the second input transistor (T_{input_2}) is coupled to the output load transistor ($T_{\text{output_load}}$). As shown, the first input transistor (T_{input_1}) and the rectifying transistor (T_{rectify}) are coupled to the current source transistor ($T_{\text{current_source}}$) and to the first input load transistor ($T_{\text{input_load}_1}$) and the second
10 input transistor (T_{input_2}) is coupled to the current source transistor ($T_{\text{current_source}}$) and to the second input load transistor ($T_{\text{input_load}_2}$). The current produced by the current source ($T_{\text{current_source}}$) flows through the first and second input load transistors based on the voltages at the gates of the first, second, and rectifying transistors. The amount of current flowing through the first input load transistor ($T_{\text{input_load}_1}$) establishes the input for
15 the transconductance (G_m) stage 118, which provides the peak value 114 of the signal 108.

To understand the operation of the rectifying operational amplifier 102, it is helpful to first discuss the operation of a conventional operational amplifier. Such a
20 conventional operational amplifier includes the current source ($T_{\text{current_source}}$), the first and second input transistors (T_{input_1}) and (T_{input_2}), and the first and second load transistors ($T_{\text{input_load}_1}$) and ($T_{\text{input_load}_2}$). Assume that the gate of the second input transistor (T_{input_2}) receives a reference voltage, which may be one-half of the supply voltage, and the first input transistor (T_{input_1}) receives the input signal. In this instance, as the voltage
25 of the input signal varies with respect to the reference voltage, the current of the current source will be proportionally provided to the first and second load transistors. For example, when the voltage of the input signal is less than the reference voltage, the first input transistor will turn on harder, thus drawing more current from the current source, which increases the current through the first load transistor. As the current through the
30 first load transistor increases, so does the output of the operational amplifier, which may be the input to the G_m stage 118. As a further example, when the voltage of the input

signal is greater than the reference voltage, the first input transistor turns on less, thus drawing less current from the current source, which increases the current through the second load transistor and decreases the current through the first load transistor. With reduced current in the first load transistor, the output of the operational amplifier is reduced. When the voltage of the input signal is of a sufficient value, all of the current produced by the current source will flow through the first load transistor or the second load transistor, producing a maximum or minimum output of the operational amplifier.

With the addition of the rectifying transistor (T_{rectify}), the current through the first load transistor ($T_{\text{input_load_1}}$) does not fall below a certain level. For example, when the gate voltage of the first input transistor ($T_{\text{input_1}}$) is less than the voltage of the second input transistor ($T_{\text{input_2}}$) and less than the voltage on the gate of the rectifying transistor (T_{rectify}), the first input transistor is on more, thus drawing more current from the current source than the second input transistor, which increases the current through the first load transistor. With more current through the first load transistor, the input to the Gm stage 118 is increased, thus increasing the output of the rectifying operational amplifier 102. When the gate voltage of the first input transistor is greater than the voltage of the second transistor and greater than the voltage on the gate of the rectifying transistor, the rectifying transistor draws a fixed level of current from the current source, which is based on its gate voltage. Since the rectifying transistor is drawing a fixed amount of current, the current through the second input transistor will be limited by the current drawn by the rectifying transistor regardless of how much more the voltage on the gate of the first input transistor increases. Thus, when the first load transistor will receive the current from the rectifying transistor, which effectively rectifies the output produced by the rectifying amplifier. Thus, in operation, the rectifying operational amplifier 102 produces the peak value 114 based on the first input 110 and the rectifying input 112, which yields an accurate, flexible (e.g., handles single-ended and differential signals equally well), and compact peak detection circuit.

Figure 4 is a schematic block diagram of the peak detection circuit 95 that is operably coupled to measure the signal strength of a single-ended version of the signal

108. In this embodiment, the input coupling circuit 100 includes two capacitors C2 and C3 and a resistor R1. The rectifying input 112 is coupled to an AC ground 130 and the first input 112 is a filtered representation, with respect to AC ground, of the signal 108. The functionality of the rectifying operational amplifier 102 is as described with
5 reference to Figure 3 and produces a half-wave rectified output. As further illustrated in this embodiment, the transconductance stage 118 include a transistor T1 and a low pass filter, which includes capacitor C4 and resistor R2.

The operation of the peak detection circuit of Figure 4 may be better described
10 with simultaneous reference to Figure 6, which illustrates the signal waveforms of the peak detection circuit. As shown in Figure 6, the signal 108 may be a sinusoidal signal. As one of average skill in the art will appreciate, signal 108 will most likely be a composition of multiple sinusoidal signals that represent an RF signal, however, for the purposes of illustration, a pure sinusoid signal will be used. With reference to Figure 4,
15 the first input 110 substantially matches the signal 108 with any high frequency components filtered via the input coupling circuit. AC ground 130 corresponds to the cross over point of the signal 108. Thus, when the signal 108 is positive, the first input 110 is positive providing a voltage above the AC ground to the gate of the first input transistor (T_{input_1}). With the gate voltage of the first transistor being greater than the gate
20 voltage of the rectifying transistor, current from the current source will flow through the rectifying transistor at a fixed level. When the signal 108 is negative, the gate voltage of the first input transistor is less than the gate voltage of the rectifying transistor, thus the current drawn from the current source will map the gate voltage of the first input transistor. Thus, the signal 108 is half-wave rectified, which, in Figure 6, is illustrated as
25 the half-wave rectified peak value 114, where the non-constant portion corresponds to when the first input transistor is drawing current from the current source and the constant portion corresponds to when the rectifying transistor is drawing a fixed current from the current source.

30 Figure 5 is a schematic block diagram of the peak detection circuit 95 that is operably coupled to measure the signal strength of a differential version of the signal 108.

In this embodiment, the input coupling circuit 100 includes three capacitors C2, C5 and C_{CM}, and two resistors R1 and R3. The center tap of resistors R1 and R3 is coupled to a common mode voltage reference (CM_{ref}), which may be AC ground. Capacitor C2 receives the positive leg of the differential signal 108-P and capacitor C5 receives the negative leg of the differential signal 108-N. The combination of resistors and capacitors of the input coupling circuit 100 filter and scale the differential input signal 108. As is illustrated, the filtered positive leg 108-P is provided as the first input 110 and the filtered negative leg 108-N is provided as the rectified input 112.

As further illustrated in this embodiment, the transconductance stage 118 include a transistor T1 and a low pass filter, which includes capacitor C4 and resistor R2. As is also illustrated, the charge pump 106 includes two transistors to produce the corresponding current 122.

The operation of the peak detection circuit of Figure 5 may be better described with simultaneous reference to Figure 7, which illustrates the signal waveforms of the peak detection circuit. As shown in Figure 7, the signal 108 may be a sinusoidal signal. As one of average skill in the art will appreciate, signal 108 will most likely be a composition of multiple sinusoidal signals that represent an RF signal, however, for the purposes of illustration, a pure sinusoid signal will be used. With reference to Figure 5, the first input 110 substantially matches the positive leg of signal 108-P with any high frequency components filtered via the input coupling circuit and the rectified input 112 substantially matches the negative leg of signal 108-N with any high frequency components filtered. Thus, when the positive leg 108-P is greater than the negative leg 108-N, the voltage to the gate of the first input transistor (T_{input_1}) is greater than the gate voltage of the rectifying transistor. With the gate voltage of the first transistor being greater than the gate voltage of the rectifying transistor, current from the current source will flow through the rectifying transistor at a level corresponding to the voltage of the rectified input 112, which corresponds to the negative leg 108-N. When the positive leg 108-P is less than the negative leg 108-N, the gate voltage of the first input transistor is less than the gate voltage of the rectifying transistor, thus the current drawn from the

current source will map the gate voltage of the first input transistor. Thus, the signal 108 is full-wave rectified, which, in Figure 7, is illustrated as the full-wave rectified peak value 114, where the even pulses result when the negative leg 108-N is greater than the positive leg 108-P and the odd numbered pulses result when the negative leg 108-N is less than the positive leg 108-P.

As one of average skill in the art will appreciate, the term “substantially” or “approximately”, as may be used herein, provides an industry-accepted tolerance to its corresponding term. Such an industry-accepted tolerance ranges from less than one percent to twenty percent and corresponds to, but is not limited to, component values, integrated circuit process variations, temperature variations, rise and fall times, and/or thermal noise. As one of average skill in the art will further appreciate, the term “operably coupled”, as may be used herein, includes direct coupling and indirect coupling via another component, element, circuit, or module where, for indirect coupling, the intervening component, element, circuit, or module does not modify the information of a signal but may adjust its current level, voltage level, and/or power level. As one of average skill in the art will also appreciate, inferred coupling (i.e., where one element is coupled to another element by inference) includes direct and indirect coupling between two elements in the same manner as “operably coupled”. As one of average skill in the art will further appreciate, the term “compares favorably”, as may be used herein, indicates that a comparison between two or more elements, items, signals, etc., provides a desired relationship. For example, when the desired relationship is that signal 1 has a greater magnitude than signal 2, a favorable comparison may be achieved when the magnitude of signal 1 is greater than that of signal 2 or when the magnitude of signal 2 is less than that of signal 1.

The preceding discussion has presented an accurate, flexible (e.g., handles single-ended and differential signals equally well), and compact peak detection circuit. As one of average skill in the art will appreciate, other embodiments may be derived from the teachings of the present invention with deviating from the scope of the claims, including, but not limited to, using N-channel transistors in place of the P-channel transistors as

illustrated in the figures and using P-channel transistors in place of the N-channel transistors as illustrated in the figures, with the power supply connections inverted.